CLAIMS:

What is claimed is:

1. A method of creating a design for a semiconductor memory, comprising:
    a. providing a leaf cell design for use by a memory compiler for a semiconductor memory, the leaf cell design further comprising a power management circuit design as a leaf cell for a memory circuit;
    b. acquiring a user input describing a parameter of a circuit, the circuit to comprise the leaf cell design;
    c. providing a user-selectable option to selectively allow enablement of an ultra low power feature; and
    d. creating a semiconductor memory design by the memory compiler which incorporates the power management circuit in a compiled semiconductor memory macro when the user-selectable option is enabled.

2. The method of claim 1, wherein the memory compiler is adapted to create a design for at least one of (1) a static random access memory, (ii) a read only memory, (iii) an embedded flash memory, or (iv) a single transistor random access memory.

3. The method of claim 1, wherein the power management circuit design is adapted to reduce leakage power resulting from a circuit resulting from use of the memory compiler.

4. The method of claim 1, wherein the power management circuit design is adapted to provide a first control voltage power supply adapted to provide power to a circuit peripheral to a memory cell array and to provide a second control voltage power supply adapted to provide power to the memory cell array.

5. The method of claim 4, wherein the power management circuit design comprises:

a. a first control supply voltage design, adapted to produce the first control voltage power supply; and

b. a second control supply voltage design, adapted to produce the second control voltage power supply;

c. wherein the second control voltage power supply is a separate voltage supply with respect to the first control voltage power supply.

6. The method of claim 5, further comprising providing the control supply voltage of the memory periphery circuit with a netlist identifier which is unique with respect to a netlist identifier for the control supply voltage of the memory cell.

7. The method of claim 5, wherein the first control voltage power supply further comprises:

a. a voltage supply; and

b. a control signal.

8. The method of claim 7, wherein the voltage supply is a variable voltage supply which may be used to provide a substantially zero voltage.

9. The method of claim 5, wherein the second control voltage supply is a variable voltage supply, further comprising:

a. allowing the second control voltage supply to operate in a minimum voltage level capable of sustaining data in the memory cell; and

b. allowing the second control voltage supply to have a substantially zero voltage in a static mode.

10. A graphical user interface, displayable on a computer display, configured to allow a user to specify a parameter for a power management circuit design as a leaf cell for a memory circuit, comprising a region of a visually perceptible display accessible by a user of a computer system, the region further comprising a user selectable option to specify selection or deselection of an ultra low power feature of power management circuit design as a leaf cell.

11. An electronic circuit created using the process of claim 1.